

This document gives details about Atlas GPIO configuration

Atlas has eight general purpose I/O lines on a pin header derived from the NM10 chipset. These I/O lines are protected with ESD devices to minimize potential damage to the NM10 from environmental conditions.

The NM10 Chipset has sixty four GPIO lines, out of it eight GPIO lines are exposed on Atlas board for users.

The following tables shows GPIO numbers mapping between NM10Chip set and Atlas board.

GPIO Numbers on Atlas Board	GPIO Number on NM10Chipset
GPIO0	24
GPIO1	26
GPIO2	27
GPIO3	28
GPIO4	33
GPIO5	34
GPIO6	38
GPIO7	39

The GPIO is mapped to base address 0x500 by BIOS.

The following registers are from NM10 chipset data sheet. Please refer Appendix for more details.

**Base + 0x07    Read/Write    Direction Register for GPIO 0, 1, 2 and 3**

Bit No.	7	6	5	4	3	2	1	0
Name				GPIO3	GPIO2	GPIO1		GPIO0

GPIO0 - 0=Output mode 1=Input mode

GPIO1 - 0=Output mode 1=Input mode

GPIO2 - 0=Output mode 1=Input mode

GPIO3 - 0=Output mode 1=Input mode

**Note:** While updating direction register, other bits 1,5,6,7 should not be changed. Read existing values and update required bits only (Use OR operation)

**Base + 0x34    Read/Write    Direction Register for GPIO 4,5, 6, and 7**

Bit No.	7	6	5	4	3	2	1	0
Name	GPIO7	GPIO6				GPIO5	GPIO4	

GPIO4 - 0=Output mode 1=Input mode

GPIO5 - 0=Output mode 1=Input mode

GPIO6 - 0=Output mode 1=Input mode

GPIO7 - 0=Output mode 1=Input mode

**Note:** While updating direction register, other bits 0,3,4,5 should not be changed. Read existing values and update required bits only (Use OR operation)

**Base + 0x0F    Read/Write    Data Register for GPIO 0, 1, 2 and 3**

Bit No.	7	6	5	4	3	2	1	0
Name				GPIO3	GPIO2	GPIO1		GPIO0

If GPIO is configured in input mode then reading this register gives the voltage status on the GPIO pin (0- 0V and 1 = 3.3V)

If GPIO is configured in output mode then writing 0 or 1 sets 0V or 3.3V respectively.

**Note:** While updating data register, other bits 1,5,6,7 should not be changed. Read existing values and update required bits only (Use OR operation)

**Base + 0x38    Read/Write    Data Register for GPIO 4, 5, 6 and 7**

Bit No.	7	6	5	4	3	2	1	0
Name	GPIO7	GPIO6				GPIO5	GPIO4	

If GPIO is configured in input mode then reading this register gives the voltage status on the GPIO pin (0- 0V and 1 = 3.3V)

If GPIO is configured in output mode then writing 0 or 1 sets 0V or 3.3V respectively.

**Note:** While updating data register, other bits 0,3,4,5 should not be changed. Read existing values and update required bits only (Use OR operation)

## Appendix

The following copied from NM10 chipset data sheet (Page no 444)

(<http://www.intel.com/Assets/PDF/datasheet/322896.pdf>)

### 13.10 General Purpose I/O Registers (D31:F0)

The control for the general purpose I/O signals is handled through a separate 64-byte I/O space. The base offset for this space is selected by the GPIOBASE register.

GPIO Register I/O Address Map

Table 13-131. Registers to Control GPIO Address Map

GPIOBASE + Offset	Mnemonic	Register Name	Default	Access
<b>General Registers</b>				
00h-03h	GPIO_USE_SEL	GPIO Use Select	1F2AF7FFh	R/W
04h-07h	GP_IO_SEL	GPIO Input/Output Select	E0E8FFFFh	R/W
08h-0Bh	—	<b>Reserved</b>	—	—
0Ch-0Fh	GP_LVL	GPIO Level for Input or Output	02FE0000h	R/W
10h-13h		<b>Reserved</b>	—	—
<b>Output Control Registers</b>				
14h-17h	—	<b>Reserved</b>	—	—
18h-1Bh	GPO_BLINK	GPIO Blink Enable	00040000h	R/W
1Ch-1Fh	—	<b>Reserved</b>	—	—
<b>Input Control Registers</b>				
20-2Bh	—	<b>Reserved</b>	—	—
2C-2Fh	GPI_INV	GPIO Signal Invert	00000000h	R/W
30h-33h	GPIO_USE_SEL2	GPIO Use Select 2 [63:32]	000300FEh	R/W
34h-37h	GP_IO_SEL2	GPIO Input/Output Select 2 [63:32]	000000F0h	R/W
38h-3Bh	GP_LVL2	GPIO Level for Input or Output 2 [63:32]	00030003h	R/W

### 13.10.1 GPIO\_USE\_SEL—GPIO Use Select Register

Offset Address: GPIOBASE + 00h      Attribute: R/W  
Default Value: 1F2AF7FFh      Size: 32-bit  
Lockable: No      Power Well: Core for 0:7, 16:23,  
Resume for 8:15, 24:31

Bit	Description
31:0	<p><b>GPIO_USE_SEL[31:0]</b> — R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function.</p> <p>0 = Signal used as native function. 1 = Signal used as a GPIO.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"><li>1. The following bits are always 1 because they are unmuxed: 6:10,12:15, 24:25</li><li>2. The following bits are not implemented because they are determined by the configuration: 16, 18, 20, 32</li><li>3. If GPIO[n] does not exist, then the bit in this register will always read as 0 and writes will have no effect.</li><li>4. After a full reset (RSMRST#) all multiplexed signals in the resume and core wells are configured as their default function. After just a PLTRST#, the GPIO in the core well are configured as their default function.</li><li>5. When configured to GPIO mode, the multiplexing logic will present the inactive state to native logic that uses the pin as an input.</li><li>6. All GPIOs are reset to the default state by CF9h reset except GPIO24</li></ol>

### 13.10.2 GP\_IO\_SEL—GPIO Input/Output Select Register

Offset Address: GPIOBASE +04h      Attribute: R/W  
Default Value: E0E8FFFFh      Size: 32-bit  
Lockable: No      Power Well: Core for 0:7, 16:23,  
Resume for 8:15, 24:31

Bit	Description
31:0	<p><b>GP_IO_SEL[31:0]</b> — R/W. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode.</p> <p>0 = Output. The corresponding GPIO signal is an output. 1 = Input. The corresponding GPIO signal is an input.</p>

### 13.10.3 GP\_LVL—GPIO Level for Input or Output Register

Offset Address:	GPIOBASE +0Ch	Attribute:	R/W
Default Value:	02FE0000h	Size:	32-bit
Lockable:	No	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	<p><b>GP_LVL[31:0]</b>— R/W: If GPIO[n] is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] bit can be updated by software to drive a high or low value on the output pin. 1 = high, 0 = low.</p> <p>If GPIO[n] is programmed as an input, then the corresponding GP_LVL bit reflects the state of the input signal (1 = high, 0 = low.) and writes will have no effect.</p> <p>When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode.</p>

### 13.10.4 GPO\_BLINK—GPO Blink Enable Register

Offset Address:	GPIOBASE +18h	Attribute:	R/W
Default Value:	00040000h	Size:	32-bit
Lockable:	No	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	<p><b>GP_BLINK[31:0]</b> — R/W. The setting of this bit has no effect if the corresponding GPIO signal is programmed as an input.</p> <p>0 = The corresponding GPIO will function normally.</p> <p>1 = If the corresponding GPIO is programmed as an output, the output signal will blink at a rate of approximately once per second. The high and low times have approximately 0.5 seconds each. The GP_LVL bit is not altered when this bit is set.</p> <p>The value of the corresponding GP_LVL bit remains unchanged during the blink process, and does not effect the blink in any way. The GP_LVL bit is not altered when programmed to blink. It will remain at its previous value.</p> <p>These bits correspond to GPIO in the Resume well. These bits revert to the default value based on RSMRST# or a write to the CF9h register (but not just on PLTRST#).</p>

### 13.10.5 GPI\_INV—GPIO Signal Invert Register

Offset Address: GPIOBASE +2Ch      Attribute: R/W  
Default Value: 00000000h      Size: 32-bit  
Lockable: No      Power Well: Core for 0:7, 16:23,  
Resume for 8:15, 24:31

Bit	Description
31:0	<p><b>GP_INV[n]</b> — R/W. <b>Input Inversion:</b> This bit only has effect if the corresponding GPIO is used as an input and used by the GPE logic, where the polarity matters. When set to 1, then the GPI is inverted as it is sent to the GPE logic that is using it. This bit has no effect on the value that is reported in the GP_LVL register.</p> <p>These bits are used to allow both active-low and active-high inputs to cause SMI# or SCI. Note that in the S0 or S1 state, the input signal must be active for at least two PCI clocks to ensure detection by the Chipset. In the S3, S4 or S5 states the input signal must be active for at least 2 RTC clocks to ensure detection. The setting of these bits has no effect if the corresponding GPIO is programmed as an output. These bits correspond to GPI that are in the resume well, and will be reset to their default values by RSMRST# or by a write to the CF9h register.</p> <p>0 = The corresponding GPI_STS bit is set when the Chipset detects the state of the input pin to be high. 1 = The corresponding GPI_STS bit is set when the Chipset detects the state of the input pin to be low.</p>

### 13.10.6 GPIO\_USE\_SEL2—GPIO Use Select 2 Register[63:32]

Offset Address: GPIOBASE +30h      Attribute: R/W  
Default Value: 000300FEh      Size: 32-bit  
Lockable: No      Power Well: CPU I/O for 17, Core for 16,  
7:0

Bit	Description
17:16, 7:0	<p><b>GPIO_USE_SEL2[49:48, 39:32] Bits[17:16, 7:0]</b>— R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function.</p> <p>0 = Signal used as native function. 1 = Signal used as a GPIO.</p> <p>After a full reset (RSMRST#), all multiplexed signals in the resume and core wells are configured as a GPIO rather than as their native function. After just a PLTRST#, the GPIO in the core well are configured as GPIO.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"><li>1. The following bits are not implemented because there is no corresponding GPIO: 31:18, 15:8.</li><li>2. The following bits are not implemented because they are determined by the configuration: 0</li></ol>

### 13.10.7 GP\_IO\_SEL2—GPIO Input/Output Select 2 Register[63:32]

Offset Address: GPIOBASE +34h      Attribute: R/W  
 Default Value: 000000F0h      Size: 32-bit  
 Lockable: No      Power Well: CPU I/O for 17, Core for 16, 7:0

Bit	Description
31:18, 15:8	Always 0. No corresponding GPIO.
17:16, 7:0	<b>GP_IO_SEL2[49:48, 39:32]</b> — R/W. 0 = GPIO signal is programmed as an output. 1 = Corresponding GPIO signal (if enabled in the GPIO_USE_SEL2 register) is programmed as an input.

### 13.10.8 GP\_LVL2—GPIO Level for Input or Output 2 Register[63:32]

Offset Address: GPIOBASE +38h      Attribute: R/W  
 Default Value: 00030003h      Size: 32-bit  
 Lockable: No      Power Well: CPU I/O for 17, Core for 16:0

Bit	Description
31:18, 15:8	<b>Reserved.</b> Read-only 0
17:16, 7:0	<b>GP_LVL[49:48, 39:32]</b> — R/W. If GPIO[n] is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] bit can be updated by software to drive a high or low value on the output pin. 1 = high, 0 = low. If GPIO[n] is programmed as an input, then the corresponding GP_LVL bit reflects the state of the input signal (1 = high, 0 = low.) and writes will have no effect. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode.